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for

BUMPING TECHNOLOGY IN STACKED DIE CONFIGURATIONS

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BUMPING TECHNOLOGY IN STACKED DIE CONFIGURATIONS

BACKGROUND OF THE INVENTION

[0001] Field of the Invention: The present invention relates to the use of bumping technology in a stacked die package. More specifically, the present invention employs bumping technology and redistribution technology to minimize a stacked die package height or to provide additional protection for the packaged die.

[0002] State of the Art: Chip-On-Board technology is used to attach semiconductor dice to a printed circuit board and includes flip chip attachment, wirebonding, and tape automated bonding ("TAB"). One example of a flip chip is a semiconductor chip that has a pattern or array of electrical terminations or bond pads spaced around an active surface of the flip chip for face down mounting of the flip chip to a substrate. Generally, such a flip chip has an active surface having one of the following electrical connection patterns: Ball Grid Array ("BGA"), wherein an array of minute solder balls is disposed on the surface of a flip chip that attaches to the substrate ("the attachment surface"); Slightly Larger than Integrated Circuit Carrier ("SLICC"), which is similar to a BGA, but has a smaller solder ball pitch and diameter than a BGA; or a Pin Grid Array ("PGA"), wherein an array of small pins extends substantially perpendicularly from the attachment surface of a flip chip. The pins conform to a specific arrangement on a printed circuit board or other substrate for attachment thereto.

[0003] With the BGA or SLICC, the arrangement of solder balls or other conductive elements on the flip chip must be a mirror-image of the connecting bond pads on the printed circuit board such that precise connection is made. The flip chip is bonded to the printed circuit board by refluxing the solder balls. The solder balls may also be replaced with a conductive polymer. With the PGA, the pin arrangement of the flip chip must be a mirror-image of the pin recesses on the printed circuit board. After insertion, the flip chip is generally bonded by soldering the pins into place. An under-fill encapsulant is generally disposed between the flip chip and the printed circuit board for environmental protection and to enhance the attachment of the flip chip to the printed circuit board. A variation of the pin-in-recess PGA is a J-lead PGA, wherein the loops of the J's are soldered to pads on the surface of the circuit board.

[0004] Wirebonding and TAB attachment generally begin with attaching a semiconductor chip to the surface of a printed circuit board with an appropriate adhesive, such as an epoxy. In wirebonding, bond wires are attached, one at a time, to each bond pad on the semiconductor chip and extend to a corresponding lead or trace end on the printed circuit board. The bond wires are generally attached through one of three industry-standard wirebonding techniques: ultrasonic bonding, thermocompression bonding and thermosonic bonding. Ultrasonic bonding uses a combination of pressure and ultrasonic vibration bursts to form a metallurgical cold weld. Thermocompression bonding uses a combination of pressure and elevated temperature to form a weld while thermosonic bonding uses a combination of pressure, elevated temperature, and ultrasonic vibration bursts. With TAB, ends of metal leads carried on an insulating tape, such as a polyimide, are respectively attached to the bond pads on the semiconductor chip and to the lead or trace ends on the printed circuit board. An encapsulant is generally used to cover the bond wires and metal tape leads to prevent contamination.

[0005] Higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits are ongoing goals of the semiconductor industry. Greater integrated circuit density is primarily limited by the space available for mounting dice on a substrate such as a printed circuit board. One way to achieve greater integrated circuit density is by attaching two or more semiconductor dice or chips in a single semiconductor assembly. Such devices are generally known as multi-chip modules ("MCM").

[0006] To further increase integrated circuit density, semiconductor dice can be stacked vertically. For example, dice may be stacked vertically on opposite sides of a substrate, or atop each other with intervening insulative layers, prior to encapsulation. U.S. Pat. No. 5,012,323, issued Apr. 30, 1991 to Farnworth, teaches combining a pair of dice mounted on opposing sides of a lead frame. An upper, smaller die is back-bonded to the upper surface of the leads of the lead frame via a first adhesively coated, insulated film layer. A lower, larger die is face-bonded to the lower lead frame die-bonding region via a second, adhesively coated, insulative film layer. The wirebonding pads on both upper die and lower die are interconnected with the ends of their associated lead extensions with gold or aluminum bond wires. The lower die must be slightly larger than the upper die such that

the die pads are accessible from above through a bonding window in the lead frame such that gold wire connections can be made to the lead extensions.

[0007] U.S. Pat. No. 5,291,061, issued March 1, 1994 to Ball ("Ball"), teaches a multiple stacked dice device containing up to four stacked dice supported on a die-attach paddle of a lead frame, the assembly not exceeding the height of current single die packages, and wherein the bond pads of each die are wirebonded to lead fingers. The low profile of the device is achieved by close-tolerance stacking which is made possible by a low-loop-profile wirebonding operation and thin adhesive layers between the stacked dice. However, Ball requires long bond wires to electrically connect the stacked dice to the lead frame. These long bond wires increase resistance and may result in bond wire sweep during encapsulation.

[0008] U.S. Patent No. 6,222,265 issued April 24, 2001 to Akram et al. teaches a stacked multi-substrate device using flip chips and chip on board assembly techniques in which all chips are wire bonded to a substrate. Further, columnar electrical connections attach a base substrate to a stacked substrate.

[0009] U.S. Patent No. 5,952,725 issued September 14, 1999 to Ball teaches a stacked semiconductor device having wafers attached back to back via adhesive. The upper wafer can be attached to a substrate by wire bonding or tape automated bonding. Alternatively, the upper wafer can be attached to a lead frame or substrate, located above the wafer, by flip chip attachment.

[0010] Several drawbacks exist with conventional die stacking techniques. As shown in FIG. 1, the top semiconductor die 12 of a semiconductor die stack assembly 10 is typically wire bonded 14 to a substrate 16. With wire bonding, the encapsulant 17 must accommodate the wire loops increasing the overall package height 18. Further, with wire bonding, a chance of electrical performance problems or shorting exists if the various wires loops come too close to each other. The wire loops can also get swept during packaging causing further electrical problems. Flip chip attachment overcomes some of these limitations. However, die stacking that relies on flip chip attachment requires the stacked die to be manufactured and vertically aligned to bring complimentary circuitry into perpendicular alignment with a lower die.

[0011] Similarly, as shown in one configuration known to the inventor herein (FIG. 6), a top semiconductor die 640 is stacked above a smaller bottom semiconductor die 620 in an active

surface 622 to backside 674 arrangement. Peripheral edges 664, 666 of the larger top semiconductor die 640 extend laterally beyond peripheral edges 660, 662 of the bottom semiconductor die 620. Similarly, a stacked board on chip assembly 700 is shown in FIG. 7 wherein a top semiconductor die 740 is stacked above a smaller, bottom, semiconductor die 720 in a backside 724 to backside 746 arrangement. The peripheral edges 764, 766 of the larger top semiconductor die 740 extend laterally beyond the peripheral edges 760, 762 of the smaller bottom semiconductor die 720. FIG. 8 illustrates a configuration known to the inventor herein depicting multiple devices on a substrate wherein each device includes two semiconductor dice in a laterally staggered arrangement. One peripheral edge 866 of a top semiconductor die 840 extends laterally beyond a corresponding peripheral edge 862 of a bottom semiconductor die 820. In FIGs. 6, 7 and 8, the top semiconductor dice 640, 740, 840 and the bottom semiconductor dice 620, 720, 820 are electrically connected to a substrate 630, 730, 830 via bond wires 628, 728, 828 that protrude above the uppermost semiconductor dice thereof, thus necessitating a higher package height 648, 748, 848.

[0012] Therefore, it would be advantageous to develop a stacking technique and assembly for increasing integrated circuit density while either decreasing the overall package height or providing additional protection for the packaged die without increasing the package height and without the necessity of altering the fabrication of the stacked die for flip-chip alignment and attachment.

BRIEF SUMMARY OF THE INVENTION

[0013] The present invention includes a stacked semiconductor assembly having a minimized package height, while providing protection for intermediate conductive elements that extend between the uppermost semiconductor die thereof and the substrate, and a method of making the same. The assembly includes a first semiconductor die having an active surface and a backside. The active surface includes a plurality of bond pads and a redistribution bond pad circuit thereon. The plurality of bond pads are electrically connected to integrated circuitry of the first semiconductor die, while the redistribution bond pads of the redistribution bond pad circuit are independent and, thus, electrically isolated from the integrated circuitry. Each redistribution bond pad circuit includes a first redistribution bond pad, a second redistribution bond pad positioned adjacent a periphery of

the first semiconductor die, and a conductive trace extending between and electrically connecting the first redistribution bond pad and the second redistribution bond pad. The first semiconductor die may be disposed directly on a substrate or a plurality of additional die may be vertically stacked on the substrate and beneath the first semiconductor die.

[0014] A second semiconductor die having an active surface and a backside is disposed above the first semiconductor die such that the active surfaces of both dice are facing one another. The active surface of the second semiconductor die includes a plurality of bond pads thereon. At least one electrical connector extends between at least one bond pad of the plurality of bond pads on the active surface of the second semiconductor die and at least one corresponding redistribution bond pad of the plurality of redistribution bond pads on the first semiconductor die. The electrical connector also spaces the active surface of the second semiconductor die apart from the active surface of the first semiconductor die a sufficient distance that bond wires or other discrete conductive elements protruding above an active surface of the first semiconductor die are electrically isolated from the active surface of the second semiconductor die and/or are not collapsed onto one another or bent, kinked or otherwise distorted by the second semiconductor die. Intermediate connective elements electrically connect the second semiconductor die and a substrate by extending from a second redistribution bond pad to a bond pad on the substrate.

[0015] Another embodiment of the invention includes a stacked semiconductor assembly, and a method of making the same, wherein the top semiconductor die of the stack has peripheral edges that extend beyond the outer periphery of the immediately underlying semiconductor die. The backside of the lower semiconductor die is secured to a substrate or another semiconductor die or stack of semiconductor dice that are secured to a substrate.

[0016] The top semiconductor die is placed above the next lower semiconductor die in an active surface-to-active surface arrangement, with at least a portion of the active surface of the top semiconductor die being exposed beyond the outer periphery of the next lower semiconductor die. At least one electrical connector extends between at least one bond pad on the active surface of the top semiconductor die and at least one bond pad on the substrate to electrically connect the top semiconductor die to the substrate.

[0017] Other features and advantages of the present invention will become apparent to those of ordinary skill in the art through consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0018] In the drawings, which illustrate exemplary embodiments for carrying out the invention:

[0019] FIG. 1 is a side cross-sectional view of a prior art stacked semiconductor device that includes bond wires connecting bond pads of both top and bottom dice to a corresponding contact area of a substrate;

[0020] FIG. 2 is a cross-sectional view of an embodiment for a vertically stacked assembly according to the invention;

[0021] FIG. 3 is a top view of a semiconductor die including a redistribution circuit on an active surface thereof;

[0022] FIG. 4 is a partial cross-section view of a redistribution circuit on a semiconductor die;

[0023] FIG. 5 is a cross-sectional view of an embodiment of a vertically stacked assembly including five semiconductor devices;

[0024] FIG. 6 is a cross-sectional view of a stacked semiconductor device that includes bond wires connecting top and bottom dice to a corresponding contact area of a substrate;

[0025] FIG. 7 is a cross-sectional view of a stacked semiconductor die assembly that include bond wires electrically connecting bond pads of both top and bottom dice to a corresponding contact area of a substrate;

[0026] FIG. 8 is a cross-sectional view of a laterally staggered semiconductor die assembly;

[0027] FIG. 9 is a cross-sectional view of an embodiment for a stacked assembly wherein the stacked dice are different sizes;

[0028] FIG. 10 is a cross-sectional view of an embodiment for a lead on chip and stacked semiconductor die combination;

[0029] FIG. 11 is a cross-sectional view of an embodiment for a laterally staggered semiconductor die assembly;

[0030] FIG. 12 is a top view of a semiconductor die according to an embodiment of the present invention;

[0031] FIG. 13 is a cross-sectional view of an embodiment for a stacked assembly wherein the stacked dice are different sizes;

[0032] FIG. 14 is a cross-sectional view of an embodiment for a laterally stacked assembly of the present invention; and

[0033] FIG. 15 is a cross-sectional view of an embodiment for a stacked assembly wherein the top semiconductor die is a leads over chip type semiconductor device with centrally located bond pads.

DETAILED DESCRIPTION OF THE INVENTION

[0034] The present invention provides a stacked semiconductor package having a reduced package height or providing additional protection for the packaged elements without increasing the package height. As shown in FIG. 2, a stacked semiconductor assembly 100 according to the present invention includes a first semiconductor die 20 having an active surface 22 and a backside 24. In FIG. 2, the first semiconductor die 20 is shown attached to a substrate 30. Although the substrate 30 is depicted as comprising a circuit board, other types of substrates including, without limitation, interposers, other semiconductor devices and leads are also within the scope of the present invention. However, as discussed herein, additional semiconductor die may be stacked between the first semiconductor die 20 and the substrate 30. A layer or film dielectric or insulative material 26 may be positioned between the active surface 22 of the first semiconductor die 20 and the active surface 46 of a second semiconductor die 40, such material may include an adhesive on one or both sides to facilitate assembly, or may comprise an electrically nonconductive adhesive to secure first semiconductor die 20 and second semiconductor die 40 to one another. In FIG. 2, the first semiconductor die 20 and second semiconductor die 40 are approximately the same size and the edges 60, 62 of the first semiconductor 20 and the edges 64, 66 of the second semiconductor die 40

are substantially aligned. Alternatively, the second semiconductor die 40 could be larger or smaller than the first semiconductor die 20.

[0035] A plurality of discrete conductive elements 28, in the form of the illustrated bond wires 28, TAB elements, leads or the like, extend from bond pads 32 (FIG. 3) on the first semiconductor die 20 to contact areas (not shown) of the substrate 30. FIG. 3 depicts a top view of the active surface 22 of the first semiconductor die 20. Thus, components common to FIGs. 2 and 3 retain the same numeric designation. Referring to FIG. 3, the first semiconductor die 20 includes a plurality of bond pads 32 on the active surface 22 thereof, which are connected to integrated circuitry (not shown) of the first semiconductor die 20. In addition, the first semiconductor die 20 includes redistribution circuits 34, each of which includes a first redistribution bond pad 36 and a second redistribution bond pad 38 that is electrically connected to the first redistribution bond pad 36 by way of a conductive trace 37 extending therebetween. Each first redistribution bond pad 36 is located so as to align with a corresponding bond pad on the active surface 46 of the second semiconductor die 40 (not shown) upon positioning the second semiconductor die 40 in inverted orientation over the first semiconductor die 20. The second redistribution bond pad 38 may be located along the outer periphery of the first semiconductor die 20 to facilitate electrical connection of the second redistribution pads 38 to corresponding contact areas (not shown) of the substrate 30.

[0036] The redistribution circuit 34 is not connected to the integrated circuitry of the first semiconductor die 20. The redistribution circuit 34, including the first redistribution bond pad 36, and the second redistribution bond pad 38, may be fabricated using redistribution technology, for example, so-called under bump metallurgy ("UBM") techniques. However, unlike current UBM techniques, the current invention redistributes substantially centrally located bond pads to the periphery of a semiconductor die. Further, unlike traditional UBM, the redistributed bond pads are not electrically connected to the semiconductor die.

[0037] Conductive traces 37 may be formed, by any method known in the art, to electrically connect first redistribution bond pads 36 with second redistribution bond pads 38. FIG. 4 depicts one exemplary method of creating the redistribution circuit 34 on a substrate 410. Pad redistribution using under bump metallurgy may be performed by depositing an optional passivation layer 420, which may comprise nitride or silicon nitride, over a substrate 410 having bond pads 430 thereon.

The passivation layer 420 is either etched or selectively deposited to allow electrical connections to be made to the bond pads 430. A dielectric layer 440, which may be formed from polyimide or benzocyclobutene ("BCB"), is deposited on the passivation layer 420. A thin film metal layer, such as titanium, copper, aluminum, NiV and/or nickel, is deposited (e.g., by sputtering) on the dielectric layer 440 and then etched to form a metal trace 450. A second dielectric layer 460 is deposited and etched to reveal a second terminal via exposing a second, connected, bond pad 470. Thus, as shown in FIG. 3, each first redistribution bond pad 36 on a first part of the active surface 22, is electrically connected to a second redistribution bond pad 38 on a second part of the active surface 22. Referring to FIG. 4, electrical connections may be made to both second redistribution bond pads 470 or first redistribution bond pads 430.

[0038] Typically, under bump metallurgy is used to reroute peripheral bond pads on a semiconductor to a different location on the semiconductor surface. The industry continues to increase the number of number of devices on a substrate, thus necessitating an increase in bond pads for each device. At a point, the bond pads become too small to economically manufacture solder balls to be small enough to fit thereon. Thus, in order to accommodate decreasing perimeter bond pad pitch, bond pads will be redistributed to other parts of the substrate. Accordingly, while FIG. 3 depicts the bond pads 32 of the first semiconductor 20 located along the outer perimeter of the active surface 22, it is understood that the bond pads 32 may be redistributed to another part of the active surface 22. Additionally, it will be understood that the top semiconductor die of any embodiment of the invention may include a redistribution circuit thereon.

[0039] The active surface 46 of the second semiconductor die 40 has bond pads arranged in a mirror image of the complementary first redistribution bond pads 36 on the first semiconductor die 20. The second semiconductor die 40 can be electrically connected to the first redistribution bond pads 36 by an electrical connector 44 extending from at least one bond pad 42 on the active surface 46 of the second semiconductor die 40 to a first redistribution bond pad 36 on the active surface 22 of the first semiconductor die 20. (FIG. 2). The electrical connector 44 and the insulative material 26 space the active surface 46 of the second semiconductor die 40 from the active surface 22 of the first semiconductor die 20. The electrical connector 44 may be a pillar bump such as the type manufactured by Focus Interconnect. However, any electrical connection known in the art is

sufficient. Pillar bumps typically include a copper base with eutectic solder caps for facilitating connection thereof to bond pads. By way of example, the height for the pillar bump may be between 95 μm and 200μm. As seen in FIG. 3, discrete conductive elements 28, such as bond wires, may extend from the second redistribution bond pad 38, thus, electrically connecting bond pads 42 of the second semiconductor die 40, corresponding redistribution circuits 34 and corresponding contact areas (not shown) of the substrate 30.

[0040] If desired, the stacked semiconductor assembly 100 may be encapsulated with an encapsulating material 70, such as silicone or epoxy, to form an encapsulated stacked semiconductor assembly 100. As seen by comparing FIG. 1 and FIG. 2, by eliminating the need for wire bonds to the top semiconductor die, the overall package height (18, 48) may be reduced. Alternatively, if the package height is maintained, the present invention provides increased protection between the wire bonds 28 and the edges of the encapsulating material 70. Further, the elimination of long bond wires 14 between a top semiconductor 12 and a substrate 16 results in less static and a decreased chance of wire sweep during packaging. A plurality of external solder balls 72 are used for electrical connection of the stacked semiconductor assembly 100 to another assembly such as a printed circuit board (not shown).

[0041] In another embodiment, the first semiconductor die 20' is not disposed directly on the substrate 30'. (FIG. 5). Instead, one or more additional dice are stacked vertically on the substrate 30'. The second surface 24' of a bottom semiconductor die 50' is placed directly on the substrate 30'. Additional dice 50" are vertically stacked above the bottom semiconductor die 50' in an active surface 54" to backside 52" arrangement. Insulative material 26' is placed between each vertically stacked die. Each semiconductor die is electrically attached to the substrate 30', by way of discrete conductive elements 28' such as bond wires, TAB elements, leads or the like. In FIG. 5, the first semiconductor die 20' is the last semiconductor die mounted in an active surface 54" to backside 24' configuration. The second semiconductor die 40' is inverted and mounted above the first semiconductor die 20' such that the active surface 46' of the second semiconductor die 40' is facing the active surface 22' of the first semiconductor die 20'. The active surface 22' of the first semiconductor die 20' includes a redistribution bond pad circuit (not shown), as described herein and depicted in FIG. 3. Thus, electrical connector 44' connects the second semiconductor die 40' to the

redistribution circuit and discrete conductive elements 28' connect the redistribution circuit and the substrate 30'.

[0042] Another embodiment of the invention provides a stacked semiconductor assembly wherein the edges of at least two of the semiconductor die are not aligned. (FIGs. 9, 10, 11). As depicted in FIG. 9, a stacked semiconductor package 900 according to the present invention, is provided with a reduced package height 948 or with additional space between electrical connections and the encapsulating material without adding any height to the package. The stacked semiconductor package 900 includes a substrate 930 that includes conductive terminal pads and corresponding traces (not shown) and has at least two semiconductor dice 920, 940 disposed thereon. At least one peripheral edge 964, 966 of the top semiconductor die 940 extends laterally beyond at least one edge 960, 962 of a bottom semiconductor die 920. The top semiconductor die 940 has an active surface 946 facing the active surface 922 of the bottom semiconductor die 920. The bottom semiconductor die 920 may be disposed directly on a substrate 930, as shown, or may be stacked above at least one other die (not shown). Bond pads 936 of the bottom semiconductor die 920 may be electrically connected to the corresponding terminals 968 of the substrate 930, by way of discrete conductive elements 928. An electrical connector 944, such as a pillar column, bump, or ball of conductive material (e.g., solder, other metal, conductive or conductor filled epoxy, anistropically discrete conductive elements 928". An electrical connector 944", such as a pillar column, bump, or ball of conductive material (e.g., solder, other metal, conductive or conductor filled epoxy, anistropically discrete conductive elements 928'". A first electrical connector 944'", such as a pillar column, bump, or ball of conductive material (e.g., solder, other metal, conductive or conductor filled epoxy, anistropically conductive elastomer, etc.), extends from a bond pad 942'" on the active surface 946'" of the top semiconductor die 940'" to its corresponding bond pad 936'" on the bottom semiconductor die 920'". The active surface 922'" of the bottom semiconductor die 920'" may include a redistribution circuit as depicted in FIG. 3 and described herein. A second electrical connector 944'" extends from a bond pad 942'" on the active surface 946'" of the top semiconductor die 940'" to its corresponding terminals 968'" of the substrate 930'".

[0043] The stacked semiconductor package 900' of FIG. 10 is similar to the stacked semiconductor package 900 depicted in FIG. 9. The stacked semiconductor package 900' includes

a substrate 930' that includes conductive terminal pads 968' and discrete conductive elements 928' and has at least two semiconductor dice 920', 940' disposed thereon. At least one peripheral edge 964', 966' of the top semiconductor die 940' extends laterally beyond at least one peripheral edge 960', 962' of a bottom semiconductor die 920'. In FIG. 10, the top semiconductor die 940' has an active surface 946' that faces the backside 924' of the bottom semiconductor die 920'. The bottom semiconductor die 920' may be disposed directly on a substrate 930', as shown, or may be stacked above at least one other semiconductor die. FIG. 10 depicts the bottom semiconductor die 920' as a LOC die with bond wires extending through an aperture in the substrate 930'. As shown, discrete conductive elements 928' may extend through an aperture 980' formed through the substrate 930' and connect bond pads 932' on the bottom semiconductor die 920' to corresponding terminals 968' on an opposite surface of the substrate 930'. Bond pads 932' of the bottom semiconductor die 920' may be electrically connected to corresponding terminal pads 968' of the substrate 930', by way of discrete conductive elements 928'. An electrical connector 944', such as a pillar column, bump, or ball of conductive material (e.g., solder, other metal, conductive or conductor filled epoxy, anistropically conductive elastomer, etc.), extends from a bond pad 942' on the active surface 946' of the top semiconductor die 940' to the corresponding terminal pad 974' of the substrate 930'.

[0044] Referring to FIG. 11, stacked semiconductor package 1000 includes a substrate 1030 having a plurality of stacked multi-chip modules 1078 thereon. Each multi-chip module 1078 includes at least two semiconductor dice 1020, 1040. At least one peripheral edge 1064, 1066 of a top semiconductor die 1040 extends beyond at least one peripheral edge 1060, 1062 of a lower semiconductor die 1020. In FIG. 11, the top semiconductor die 1040 has an active surface 1046 that faces the active surface 1022 of the bottom semiconductor die 1020. As shown in FIG. 11, the active surface 1046 of the top semiconductor die 1040 may have unobstructed access to an underlying substrate 1030. If the area between the active surface 1046 of the top semiconductor die 1040 and an underlying substrate 1030 is obstructed by a die, or other object, that die or object can include a redistribution circuit as discussed herein.

[0045] The bottom semiconductor die 1020 may be disposed directly on a substrate 1030, as shown, or may be stacked above at least one other die (not shown). The bottom semiconductor die 1020 can be electrically connected to the substrate 1030, by way of discrete conductive elements

1028. An electrical connector 1044, such as a pillar column, bump, or ball of conductive material (e.g., solder, other metal, conductive or conductor filled epoxy, anistropically conductive elastomer, etc.), extends from a bond pad 1042 on the active surface 1046 of the top semiconductor die 1040 to a corresponding terminal pad 1074 of the substrate 1030. An insulative layer 1026 may be disposed between the top semiconductor die 1040 and the bottom semiconductor die 1020. The multi-chip modules 1078 may be encapsulated either individually or as a group as shown in FIG. 11.

[0046] Another embodiment is shown in FIG. 15 wherein the top semiconductor die 1540 is an LOC-type semiconductor device with centrally located bond pads 1542. At least one electrical connector 1544 extends from bond pads 1542 on the top semiconductor die 1540 to corresponding bond pads 1532 on the bottom semiconductor die 1520, as shown, or to corresponding terminal pads on the substrate 1530 (not shown). The bottom semiconductor die 1520 may include redistribution circuits as shown in FIG. 3 and described herein.

[0047] Although the foregoing description contains many specifics, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some exemplary embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. Features from different embodiments may be employed in combination. The scope of the invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions, and modifications to the invention, as disclosed herein, which fall within the meaning and scope of the claims are to be embraced thereby.